

METHOD AND APPARATUS FOR IDENTIFYING A VERTICAL BLANKING
INTERVAL IN A TELEVISION SIGNAL

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BACKGROUND OF THE INVENTION

The present invention relates to television (TV) anti-copy protection (ACP) processes as well as to processes for defeating or reducing the effects of copy protection signals and, more particularly, to various unconventional techniques for identifying the occurrence of the vertical blanking interval (VBI) in a television signal. This information is required in copy protection defeating processes which need to locate the VBI in order to remove any of the various types of copy protection signals that conventionally are inserted in various video lines in the VBI. The invention further relates to techniques for defeating the processes of identifying the VBI, that is, for preventing the identification of the VBI via the unconventional techniques disclosed herein.

In the television field, the development of copy protection processes for protecting television signals recorded on various recording mediums or transmitted over various transmission mediums, has resulted in the proliferation of schemes and devices for locating and then removing the copy protection signals from the TV signals in order to illegally copy the recorded or transmitted signal for profit. Typical of such devices for defeating copy protection processes are those known colloquially as "black boxes."

Various types of illegal black boxes are effective in neutralizing respective types of copy protection (or scrambled) signals such as those using for example, pseudo sync/AGC pulse manipulation, horizontal or vertical sync suppression and/or modulation, color burst manipulation, etc., techniques. In most such types of illegal black boxes it first is necessary to locate a reliable vertical sync or vertical rate signal. Once a reliable vertical related signal is established, circuits such as sync separators and low pass filters deliver timing signals which in turn enables the defeat of the copy protection signals and the generation of a viewable video signal. In a typical technique, circuits are used to identify the characteristically longer broad vertical sync pulses to generate a vertical (or frame) rate signal. In a further technique, black boxes utilize the color burst signal in the television signal to attain illegal decoding, wherein the lack of color burst in conventional lines of the VBI can be detected to thereby identify the VBI and enable the illegal generation of a reliable vertical rate signal.

In a still further type of black box technique, a computer is used to analyze a video signal to determine the location of the VBI and generation of a vertical related signal, thereby enabling the illegal decoding of the copy protection signal.

SUMMARY OF THE INVENTION

Accordingly, it would be highly desirable to explore all possible alternative unconventional techniques for identifying a VBI and thus for generating a reliable vertical and/or frame rate signal based on a video input signal such as, for example, standard, scrambled and copy protected video signals.

To this end, the present invention provides various embodiments of methods and apparatuses for identifying a VBI employing unconventional techniques based upon the peculiarities and specific characteristics of the video line waveforms within the vertical blanking interval (VBI). Included in the embodiments are those enumerated here by way of
5 example only.

A first embodiment senses the time interval between certain horizontal sync edges. The time interval between normal horizontal sync pulses is 63.55 microseconds (μ s). However, in the VBI, there are pulses spaced apart about half the normal interval, or about 32 μ s. It follows that the 32 μ s spacing can be considered an indication for identifying the VBI
10 and for then generating a vertical rate pulse. A timing circuit may then be used to generate the vertical or frame rate pulse with the proper timing to modify the ACP or video signal.

Another embodiment senses a time interval of about 4.7 μ s plus 2.3 μ s, or about 7 μ s. This time interval occurs in the VBI on lines six (6) - seven (7) and on line 269 in the NTSC color video standard and upon detection can be used as a VBI indicator.

15 A further embodiment comprises measuring the pulse widths of horizontal sync signals for those pulses that are less than the normal 4.7 μ s, which narrow horizontal sync signals occur in the VBI and thus can be used as indicators of the VBI.

Another embodiment comprises generating a pulse greater than 4.7 μ s but less than about 27 μ s by triggering off the leading edge of the horizontal sync. This pulse then is used
20 to gate out sync pulses. Signals such as the broad vertical pulses forming the vertical sync signal will output pulses, whereas horizontal sync signals and/or equalizing pulses will be gated out and will not output a pulse. This condition also provides an indication of the VBI.

A further embodiment comprises measuring the time interval between the trailing edges of two pulses and then searching for a period of about $56.5\ \mu\text{s}$ which occurs once every field on video line 266 and lines three (3) - four (4) in the NTSC standard. Detection of the $56.5\ \mu\text{s}$ time interval is used as an indication of the VBI.

5 A still further embodiment includes providing an "inept" or incorrectly operated (i.e., "incorrect" for simplicity) 2H eliminator circuit that triggers off the trailing edge (rather than the leading edge) of a horizontal sync pulse (Hsync), for a non-retriggerable duration of over a half of a line ($1/2\ H$) duration (i.e. about $45\ \mu\text{s}$). The time interval as measured at the output of the "incorrect" 2H eliminator circuit between most video lines will be $63.55\ \mu\text{s}$
10 except on lines 266 and 3 - 4 (in the NTSC standard). The time interval between the leading edges of the H sync pulses on lines 3 - 4 will be about $88.3\ \mu\text{s}$ and the interval between the trailing edges of the sync pulses on line 266 is $56.5\ \mu\text{s}$. This information can be used as an indication of the VBI presence, whereby a vertical rate signal may be produced.

Another embodiment comprises sensing the pseudo sync pulses of a corresponding
15 anti-copy protection signal and measuring the time interval between these pulses, nominally less than $10\ \mu\text{s}$, to locate the VBI.

In an alternative portion of the invention, that is, where the VBI signals are modified to prevent the unconventional techniques from locating the VBI as disclosed above, further embodiments for preventing the identification of the VBI includes eliminating or modifying
20 certain pulses such as eliminating the 2H (twice horizontal) pulses in at least a part of the vertical sync signal, or adding fake 2H pulses near the bottom of the active TV field, (etc). In addition, the elimination or addition of pulses may be modulated as, for example, by AM,

position and/or pulse width modulation processes, to cause a black box to output a further degraded signal.

A third portion of the invention herein concerns the utilization of the reliable vertical rate signal produced by the first portion of the invention, which identifies the VBI by
5 unconventional techniques, to modify or otherwise reduce the effects of an anti-copy protection signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a partial diagram illustrating the waveforms of the signals in a conventional
10 vertical blanking interval (VBI), for a NTSC color video standard, further illustrating the techniques of the various embodiments of previous mention and discussion below, for sensing and determining a vertical rate signal.

FIGs. 1A and 1B are enlarged views of portions of FIG. 1 showing in further detail pertinent portions of the waveforms.

15 FIG. 2 is a block diagram illustrating a basic configuration of vertical rate signal regeneration circuitry for deriving a vertical rate signal via unconventional means in accordance with the first portion of the invention.

FIG. 3 is a block diagram illustrating embodiments of the invention which sense pulse intervals of about 32 microseconds (μ s) to produce a reliable vertical rate signal.

20 FIG. 4 is a block diagram illustrating several embodiments of the invention which sense pulse intervals of 7 μ s, about 56.5 μ s and 88 μ s, and/or sense pulse widths of about 2 μ s, and/or greater than 5 μ s.

FIG. 5 is a block diagram illustrating still other embodiments of the invention which sense pulse widths of various selected durations to derive the reliable vertical rate signal.

FIG. 6 is a block diagram illustrating in further detail several of the embodiments of the invention previously depicted for example in FIGs. 3, 4 and 5.

5 FIG. 6A is a block diagram illustrating an adjunct embodiment of the invention useful for example with the circuit of FIG. 6 in given noisy signal conditions.

FIG. 7 is a block diagram illustrating another embodiment of the invention which measures pulse widths of positive going pulses.

FIG. 8 is a block diagram illustrating a basic configuration of vertical rate signal
10 regeneration circuitry of the second portion of the invention, which is thus adapted for deriving an incorrect, i.e. unreliable, vertical rate signal; that is, for defeating or preventing the generation of a proper, i.e. reliable, vertical rate signal such as provided by the circuitry of FIG. 2, and FIGs. 3-7.

FIG. 9 is a block diagram illustrating embodiments of the basic configuration of FIG.
15 8 for defeating, that is, preventing, the generation of correct or reliable vertical rate signals.

FIG. 10 is a partial diagram of the waveforms in the VBI illustrating the addition of selected pulses in different locations of the video signal depicted in for example FIG. 1, to prevent the generation of a reliable vertical rate pulse.

FIG. 11 is a block diagram illustrating another embodiment of the second portion of
20 the invention which defeats or prevents the generation of a correct or reliable vertical rate signal.

FIG. 11A is a block diagram illustrating a further embodiment of the invention of FIG. 11, and depicting another circuit for inserting pulses or signals in the video signal to prevent generating a correct or reliable vertical rate signal.

FIG. 12 is a block diagram illustrating an embodiment of the previously mentioned
5 third portion of the invention in which reliable vertical rate signals such as generated in FIGs. 3-7 are then used to modify a selected portion(s) of an anti-copy protection signal in the VBI.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

It is to be understood that the present invention contemplates three individual yet
10 complementary portions or concepts.

First, the invention is concerned with a reliable vertical rate generation portion that derives a vertical rate signal utilizing unconventional techniques made possible by the particular characteristics and peculiarities of the VBI waveforms in conventional television signals.

15 Second, the invention is concerned with a portion that selectively modifies particular signals in the VBI of conventional television signals to prevent the derivation of a reliable vertical rate signal such as those using the unconventional techniques of the above first portion of the invention.

Third, the invention is concerned with a portion which utilizes the unconventionally
20 derived, reliable vertical rate signal of the first portion of previous mention, to then selectively modify a television signal or copy protected television signal, to reduce the effects of the copy protection signals for VCR and/or TV sets.

Considering the first portion of the invention, FIG. 1 illustrates diagrammatically several examples of pulse widths and/or pulse spacings in a conventional VBI of a NTSC color television standard, the dimensions and/or timing of which provide unconventional means for identifying the presence of the VBI. The specific examples of pulse widths and/or spacings are circled and numbered to facilitate their description in the following specification with respect to respective figures. It is to be understood that the techniques described in terms of the NTSC standard are equally applicable to the PAL, etc., standards.

FIG. 1 is further described in FIGs. 1A and 1B which show in greater detail in broken-out sections, the examples of the invention numbered #5 and #1, #3, respectively.

FIGs. 1A and 1B include legends describing in detail various pulse widths, spacings, etc., and thus are generally self explanatory taken in conjunction with FIG. 1.

FIG. 2 illustrates basic circuitry definitive of the first portion of previous mention of the invention, wherein a video signal, which can include a copy protection signal, is supplied via an input 20 to a timing circuit 22, as well as to a signal processing circuit 24. A timing signal indicative of the input sync signal is supplied by circuit 22 (which may include a sync separator) to another signal processing circuit 26. In accordance with the first portion of the invention, the processing circuit 26 includes circuit means for sensing selected pulse widths and/or pulse spacings peculiar to the VBI waveforms illustrated in FIG. 1. It follows that the output of circuit 26 is the desired reliable vertical rate signal. As depicted in phantom line, an optimal timing circuit 25 may be included to provide suitable timing for properly relocating a vertical or frame rate signal which then is used for modifying the video and/or ACP video signal, for example, in the VBI.

It is to be understood that although the embodiments of the invention are described herein as providing reliable vertical rate signals (in portion or concept 1) a reliable frame rate signal may be provided if desired, and a suitable vertical rate signal may be derived from a frame rate signal.

5 In accordance with the invention, the reliable vertical (or frame) rate signal in turn can be used in the processing circuit 24, defined previously as the third portion of the invention, to selectively modify an anti-copy protection (ACP) signal embedded in a video signal, such as the copy protected video signal depicted at input 28, to provide a modified ACP signal on output 29. It is readily apparent that the vertical rate signal generated by the circuitry 22 and
10 26 may be used in any other type of user apparatus which requires a vertical rate signal, and is not limited to use with the ACP processing circuit 24 depicted herein by way of example only.

FIG. 3 illustrates two different circuits for generating a reliable vertical rate signal in
15 accordance with the invention by sensing the period, or spacing, between positive or negative transitions from one sync pulse to another for an approximate 32 microsecond (μ s) spacing in the VBI. The 32 μ s spacings occur in the vertical sync signal such as in the pre-equalizing pulse interval, the vertical sync pulse interval or in the post equalizing pulse interval. See, the sample #1 in FIGs. 1 and 1A. To this end, in one embodiment, a video sync signal such
20 as a composite sync signal, is supplied on an input 38 to a spacing detector 40 which detects pulse transition spacings of about 32 μ s \pm 20%, wherein the transitions are positive or

negative. Thus, the spacing detector 40 provides a reliable vertical rate signal 42 via an output 42.

In another embodiment of FIG. 3, the video sync signal on input 38 is supplied to a frequency sensing circuit 44 which senses for a frequency component corresponding to about a 32 μ s period. See again the example #1 in FIGs. 1 and 1B. In FIG. 3, the video's sync pulses are primarily at a frequency of about 15.734 kilohertz (kHz). But in the VBI, there are some 31.5 kHz frequency components due to the 32 μ s spacing of edges from vertical sync signals such as equalizing pulses or serrated vertical sync pulses. The sensing circuit 44 thus includes (an optional) one-shot 46 of 16 μ s coupled to a bandpass filter 48, or equivalent, to provide a peaked response. The output of bandpass filter 48 is supplied to a threshold detector 50 which provides a reliable vertical rate signal 52 on an output 52 when 32 μ s period pulses are present. The bandpass filter 48 may have a range of 20 kHz to 45 kHz, for example. As indicated, the vertical rate signals 42 and 52 of FIG. 3 may not be the same depending upon in which portion of the VBI they are detected.

FIG. 4 illustrates several other embodiments of the invention for generating a vertical rate signal by sensing other specific edge transition spacings and/or pulse widths. In one embodiment, a video sync signal on an input 56 is supplied to a spacing detector 58 which senses for a 7 μ s spacing between leading edge transitions in video lines 6-7 and/or 269. See the example #2 in FIG. 1. Detector 58 provides a reliable vertical rate signal 60 on an output 60 upon sensing the 7 μ s spacing.

In another embodiment, the video sync signal is supplied to a spacing detector 62 which senses for about a 56.5 μ s spacing between trailing edge transitions in video lines 3-4

and/or 266. See the example #5 in FIGs. 1 and 1B. Detector 62 then provides a reliable vertical rate signal 64 on an output 64 upon sensing the 56.5 μ s spacing.

In a further embodiment of FIG. 4, a pulse width detector 66 is coupled to the video sync signal via the input 56 and detects an approximately 2 μ s pulse width, such as that of an equalizing pulse, and provides a reliable vertical rate signal 68 on an output 68 in response thereto. See example #3 in FIG. 1. The detector 66 can also receive inverted sync pulse polarities and then sense for a 4.7 μ s pulse width of a vertical serration signal, such as illustrated in FIG. 1B by an example #3A.

Another embodiment illustrated in FIG. 4 includes pulse detector circuit 70 formed of a one-shot 72 which receives an inverted video sync signal via the input 56 and an inverter 74. The one-shot 72 is coupled to an AND gate 76 via an inverter 78, and the second input to AND gate 76 is a time delayed signal from the inverter 74 via a delay circuit 80. The pulse detector circuit 70 generates a horizontal sync pulse with a width which is longer than normal, for example, which is at least 5 μ s, to thereby gate out the first 5 μ s of any sync pulse. It follows that all pulses such as equalizing pulses (of about 2 μ s), and normal horizontal sync pulses (of 4.7 μ s), will not produce an output from the AND gate 76. Only pulses longer than 5 μ s such as vertical sync pulses will produce a reliable vertical rate signal 82 via the AND gate 76 on an output 82. See the example #4 in FIG. 1.

The last embodiment of the invention illustrated in FIG. 4 comprises an "incorrect" (i.e. "inept) twice horizontal rate (2H) eliminator circuit 86. That is, the trailing edge of the video sync signal pulse is used to trigger a timing circuit formed of a one-shot 88 whose period is greater than a one-half of a horizontal line period, for example, 40 μ s. The output

of one-shot 88 is supplied to a detector 90 which senses a period of about 88 μ s and triggers off the leading edges of the pulses from the one-shot. See the example #6 in FIG. 1. It is noted that a "correct" 2H eliminator circuit triggers off a leading edge of pulses rather than the trailing edge as does the "incorrect" eliminator circuit 86, with a greater than one-half line period timing circuit, and thus produces a horizontal rate signal. The incorrect 2H eliminator circuit 86 provides a reliable vertical rate signal 92 on an output 92 in accordance with the invention. As previously mentioned, the circuits of FIG. 4 alternatively can output reliable frame rate signals instead of vertical rate signals.

The incorrect 2H eliminator circuit 86 also can generate a reliable vertical (or frame) rate signal by sensing pulse periods other than the 88 μ s periods. For example, the circuit 86 can also detect a period of about 71 μ s which occurs in the post equalization pulse interval which immediately follows the vertical sync pulse interval, in the VBI in selected lines in a field, and is an indication of the VBI occurrence. Alternatively, the circuit 86 can detect a period of about 96 μ s which occurs in the last portion of the post equalization pulse interval in the VBI of selected lines in a field, to provide a reliable vertical rate signal in accordance with the invention. In each of these examples, the incorrect 2H eliminator circuit 86 triggers off the trailing edge of the video sync signal, and the one-shot 88 has an interval of greater than one horizontal line (for example 64 μ s) but less than two horizontal lines (for example 128 μ s).

Although the VBI location technique of the invention is described herein in terms of an NTSC color television standard, it is equally applicable to other standards such as PAL, etc.

FIG. 5 illustrates still further embodiments of the invention for sensing and generating a reliable vertical (or frame) rate signal via unconventional means involving the particular characteristics of the VBI signals. In one embodiment a video sync signal is supplied via an input 96 and an inverter 98 to a pulse width detector 100 which measures the width of the positive going H sync pulses within the broad vertical sync pulses. The positive going H sync pulses are about $4.7 \mu\text{s}$ and are measured for example via an inverted H sync signal. A reliable vertical rate signal 102 is provided on an output 102. See example #3A in FIG. 1B.

In another embodiment of FIG. 5, a vertical rate signal is provided on an output 106 via a pulse width detector 104 which measures the width of a signal for a duration of about $1/2 H - 2.3 \mu\text{s}$ where H is a horizontal line period. See example #3B in FIG. 1B. This duration is found for example in horizontal lines 266 and/or 3-4, as may be seen in FIG. 1.

A further embodiment includes a pulse width detector 108 which measures the width of a vertical sync pulse, about $1/2 H - 4.7 \mu\text{s}$, and provides a reliable vertical rate signal 110 on output 110. See example #3C in FIG. 1B.

FIG. 6 illustrates in further detail some of the various embodiments of the invention of previous description in FIGs. 3-5. A video signal is supplied via an input 120 to a sync separator circuit 122, whose output is supplied to a counter 124 via an inverter 126, contacts 2, 3 of a jumper JP1 and a delay circuit 130. Sync separator 122 output also is supplied to contact 1 of the JP1 and to the input of a flip flop 132. The signal to counter 124 resets it on the leading edge of the sync pulses. At this time the contacts 1, 2 of the jumper JP2 coupled to flip flop 132 are open. Counter 124 is clocked by an oscillator circuit 128 and thus counts up to a selected number of clocks before being reset to zero on the leading edge of the next

sync pulse. Before counter 124 is edge reset to zero, the final count therein is transferred to a memory latch 134. The final counts are indicative of the period between successive leading edge transitions of the sync signal. The output from the latch 134 is then supplied to digital comparators 136, 138, 140 and 142, which provide high logic state signals (i.e., V rate

5 signals 144, 146, 148, 150) on respective outputs 144, 146, 148 and 150 based on a range of numbers set by respective threshold inputs L1-L2, L3-L4, L5-L6 and L7-L8.

By way of example, if the clock from oscillator circuit 128 is running at a $1\ \mu\text{s}$ rate, the latch 134 will output numbers of 64, 32, 56 and 7, as well as any other desired numbers. The digital comparator 136 may have its threshold inputs L1, L2 set for numbers 30 and 36

10 respectively, whereupon a count of from 30 to 36 inclusive from latch 134 would provide a high logic state on the output 144. An AND gate 145 is coupled to the output 144 and also to the contact 2 of JP1, and provides a gated signal indicative of occurrences of a $32\ \mu\text{s}$ period on an output 147.

Similarly, the digital comparator 138 may have set limits on inputs L3, L4 for

15 numbers from 5 to 9 so that a count of for example 7 would provide a high logic state on the respective output 146. The digital comparator 140 may have set limits of from 54 to 59 whereby a count of 56 or 57 causes a high logic state on the output 148. It may be seen accordingly that the digital comparators 136-140 comprise detection circuits for the $32\ \mu\text{s}$, the $7\ \mu\text{s}$ and the $56\ \mu\text{s}$ periods between successive sync edges, which periods conform to the

20 examples described previously in relation to the FIGs. 3, 4, 5 and illustrated for example in FIG. 1.

In the situation where jumper JP1 is not connected to any contact and jumper JP2 is loaded, an "incorrect" 2H eliminator circuit 152 is provided via the flip flop 132 and a counter 154. The flip flop 132 sets a high output at a trailing edge of sync. The counter 154 counts for over one-half of a video line's period (that is, 40 μ s or a count of 40 for a 1 μ s clock from oscillator circuit 128) before resetting the flip flop 132 and then also resetting itself. The output from the flip flop 132 is a pulse of a width of greater than one-half of a line's period and is supplied to the counter 124, the latch 134 and to the digital comparator 142. The latter also detects the spacing between edges of successive pulses as do the comparators 136-140. The output of the flip flop 132 is usually about 64 μ s but an 88 μ s spacing does occur at a vertical or frame frequency rate, once per VBI. Therefore the flip flop 132 provides numbers of 64 and 88 assuming that oscillator circuit 128 is running at a 1 μ s period. The digital comparator 142 is set at limits of 86 to 90 counts via the inputs L7 and L8 and thus provides a logic high state on the output 150 whenever an 88 μ s spacing occurs. See the example #6 in FIG. 1.

FIG. 6A illustrates an alternative embodiment of an adjunct circuit which may for example receive the signals on the outputs 144, 147 of FIG. 6, and which provides on an output 160 a high logic state when a minimum number of pulses of a particular spacing occurs. An inverter 162 supplies the signal on input 144 to a counter 164, wherein the latter is clocked via the gated signal on input 147. The counter 164 counts for example the number of times the 32 μ s spacings occur before being reset to zero, and supplies a resulting output to a digital comparator 166. The latter has a set limit supplied via an input L9 of for example

greater than 2, 5, etc., pulses of 32 counts or 32 μ s, whereupon it outputs a high logic state corresponding to the reliable vertical rate signal via the output 160.

The circuit of FIG. 6A is useful in certain noisy conditions where a vertical rate pulse is generated only after a particular number of pulses of the proper spacing, period or width is produced.

FIG. 7 illustrates an embodiment of the invention for measuring the pulse width of a positive going pulse. To this end, a positive going pulse is supplied via an input 168 to a delay circuit 172 via an inverter 170, which also supplies the clock input of a latch 174. The output of the delay 172 allows a counter 176 to count clocks supplied to its clock input for the duration of the positive going pulse. Before the final count is reset, latch 174 stores the last number in the counter 176. Thus the delay 172 allows the latch 174 to store the last count prior to the reset of the counter 176. The output of the latch 174 provides numbers corresponding to the pulse width of the positive going pulse. For example, if the clock to counter 176 has a period of 0.1 μ s, then a 2.3 μ s wide positive going pulse will cause a number 23 to output from the latch 174. A digital comparator 178 then receives the number(s) provided by the latch 174 and produces a logic high state on an output 180 for numbers that fall within the range of numbers, that is, limits, set at inputs L10 and L11 to the comparator 178. For example, L10 may be set at 20 and L11 may be set at 26.

As described above, the FIGs. 3-7 are concerned with the first portion of the invention of previous mention. The following FIGs. 8-11 and 11A are concerned with the second portion of the invention, also previously mentioned, which includes means for preventing the successful generation of a reliable vertical rate signal, such as when using the unconventional

techniques of the first portion of the invention which derives a vertical rate signal utilizing the particular characteristic signals in the VBI.

To this end, FIG. 8 illustrates basic circuitry of the previously mentioned second portion of the invention, wherein the VBI of a video signal or of an ACP video signal is selectively modified to prevent the use of the unconventional techniques of deriving the vertical rate signal such as those described herein with respect to the first portion of the invention of FIG. 2 and FIGs. 3-7. In FIG. 8, a video signal or ACP video signal is supplied via an input 181 to a timing circuit 182 similar to the timing circuit 22 of FIG. 2, and also to a (third) signal processing circuit 184. The timing signal from circuit 182 is supplied to the signal processing circuit 184 which in turn selectively modifies, attenuates, adds to and/or inserts into the VBI selected signals which will prevent a circuit such as processing circuit 26 of FIG. 2 from generating a correct or reliable vertical rate signal. Such selected signals are illustrated by way of example in FIG. 10. Thus, circuit 184 outputs an "incorrect" or unreliable vertical rate signal on an output 185.

FIG. 9 illustrates circuitry of an embodiment of the invention which prevents the generation of a reliable vertical rate signal such as provided for example by the techniques described above with respect to FIGs. 3-7. In FIG. 9, a video signal is supplied to a timing circuit 186 and to one input of first and second switches 188, 190 via an input 192. The second inputs of the switches 188 and 190 are supplied with selected voltages V_{b1} and V_{b2} , respectively. The timing circuit 186 supplies a first signal which identifies the locations of lines 6-7 and 269 and is used to control the switch 188 to modify the video sync pulses so that a 7 μ s spacing is substantially eliminated at selected times. Thus the technique disclosed

above, wherein a reliable vertical rate signal is generated by detecting a 7 μ s pulse in the VBI, is defeated.

The timing circuit 186 supplies a second signal which identifies the locations of video lines 3.5 and 266 and is used to control the switch 190 to modify the video sync pulses so
 5 that a 56.5 μ s spacing is substantially eliminated at selected times. This defeats the technique of previous description which senses the 56.5 μ s spacing to generate a reliable vertical rate signal.

Other embodiments may be applied to substantially eliminate or selectively modify the various edge spacings and/or pulse widths to prevent their being detected to generate a
 10 reliable vertical rate signal. For example, the V sync pulse may be sufficiently shortened or lengthened on lines 6-7 and 269 to substantially eliminate its detection, for example, for a 7 μ s spacing (example #2, FIG. 1).

FIG. 10 illustrates by way of example, the insertion of specific signals in different locations in the video signal such that these signals, for example of about 7 μ s, about 56.5 μ s
 15 and/or about 32 μ s periods similar to sync pulses, are inserted such as in locations in or near the end or beginning of the active video field. For instance, another example would be the modification of a signal near the beginning and/or end of the vertical sync signal area. (The vertical sync signal includes pre and post equalizing and broad sync pulse intervals). See the examples #7 and #8 in FIG. 10. Signals such as these may be inserted into the video signal
 20 using circuits such as those illustrated in FIG. 9.

FIG. 11 illustrates a further embodiment for modifying a video signal or an anti-copy protection (ACP) video signal so as to cause unconventional vertical rate generator or

detection circuits to fail, to behave inconsistently, or to generate vertical rate signals at the wrong time(s). In FIG. 11, a video signal is supplied via an input 198 to a sync separator circuit 200 that supplies H sync and frame signals to a timing circuit 202. The outputs of timing circuit 202 are line and pixel location signals which are then coupled to a modifier circuit 204 which also has the input video signal coupled to it. Modifier circuit 204 causes the modification of a portion or portions of the video signal by selected processes such as by deleting, inserting, attenuating, narrowing, widening, width modulating, amplitude modulating, position modulating, and/or level shifting processes. One such modifying circuit can be a signal inserting circuit for substituting different level signals for normal blanking, sync tip, etc., level signals.

By way of example, various processes for the modifications of previous mention include:

1) Modifying any combination of equalizing pulses or half line pulses. For example, modifying any combination of half line pulses in the vertical sync signal (i.e., lines 1-9 and/or lines 263 to 271 inclusive of FIG. 1). This would cause the 32 μ s detector (viz, circuits 40, 44 in FIG. 3) to output an unreliable vertical rate signal.

2) Modifying the positive going pulse at the end of line 6 and/or at the middle of line 269 so a circuit such as circuit 58, a 7 μ s spacing detector in FIG. 4, produces an unreliable vertical rate signal.

3) Modifying the negative going pulse at the beginning of line 7 and/or in the middle of line 269, so a circuit such as circuit 58, a 7 μ s spacing detector in FIG. 4, produces an unreliable output.

4) Modifying any combinations of the pre and/or post equalization pulses so as to cause a circuit such as 7 μ s spacing detector 58 in FIG. 4, to produce an unreliable output.

5) Modifying any combination of the negative going pulse at the beginning of line 266 and/or middle of line 3 so a circuit such as 56.5 μ s spacing detector 62 in FIG. 4, produces an unreliable output.

6) Modifying any combination of the positive going pulses at the middle of line 4 and/or at the end of line 266 so a circuit such as circuit 86 in FIG. 4, comprising an incorrect 2H eliminator circuit and an 88 μ s spacing detector, produces an unreliable output.

7) Modifying the video signal by selectively adding or inserting either positive and/or negative going pulses. For example, adding or inserting at least one negative going pulse in the location of the pre or post equalizing pulses will cause a 32 μ s spacing detector such as those in FIG. 3 to not work properly or reliably. In another example, adding or inserting at least one positive going pulse in the region of line 6, preferably close to the positive going pulse at the end of line 6, can cause a 7 μ s detector such as the spacing detector 58, FIG. 4, to perform unreliably. In yet another example, adding or inserting a negative going pulse during the first half line of line 266, or near the end of line 3, can cause a 56.5 μ s spacing detector, such as the detector 62 of FIG. 4, to not work reliably.

8) Furthermore it is possible to add or insert negative going pulses, modulated or not, in the area outside the VBI to cause the 32 μ s, 7 μ s, 56.5 μ s, and/or 88 μ s detectors of previous example to output a vertical rate pulse with the wrong timing, i.e., early and/or late.

9) It is also possible to narrow certain horizontal sync pulses to the duration of equalizing pulses to cause a 2 or 2.3 μ s width detector to output a signal early and/or late.

10) It is also possible to add or insert negative going pulses of the duration of an H sync pulse in the pre and/or post equalizing pulse locations, to form at least one positive going pulse of about $4.7 \mu\text{s}$ in these locations so that a $4.7 \mu\text{s}$ detector will output a signal early and/or late.

5 11) Modifying at least one equalizing pulse, such as the pulses labeled "Z" in FIG. 1, such as by attenuating, narrowing or blanking processes. Alternatively, at least one serration pulse "Z1," FIG. 1, may be modified in similar manner. One example is to remove all Z pulses.

10 12) It is also possible to provide the modification process by employing any combination of the possibilities 1-11 above.

FIG. 11A illustrates in further detail an embodiment of the modifier circuit 204 for modifying a video signal to cause the various detectors and/or vertical rate generators of for example previous mention, to output an unreliable vertical rate signal. FIG. 11A illustrates in particular a process for the insertion of signals. Input video is coupled to a switch 206 via an input 208. The switch 206 is controlled by an AND gate 210 which is logic high for selected portions of a video signal so as to allow the switch 206 to insert either negative and/or positive going pulses into the video signal. When a voltage source $V_b(t)$ applied to a second input of the switch 206 is below normal blanking level, negative going pulses are inserted and/or existing negative going pulses are widened. Alternatively, when $V_b(t)$ is at about normal blanking level, existing negative going pulses are at least narrowed and/or positive going pulses are inserted. In either situation, the video signal with modified sync pulses is output via an amplifier 212 and an output 214.

FIG. 12 illustrates another embodiment of the invention corresponding to the third portion of the invention of previous mention, in which the unconventionally derived reliable vertical rate signals of the first portion of the invention are utilized to selectively modify the video signal. To this end, FIG. 12 utilizes a reliable vertical rate signal (VID) generated by such methods as illustrated in circuits 42, 44, 58, 62, 66, 70, 86, 100, 104 and/or 108. Signal VID is coupled via an input 216 to a timing generator circuit 218 which generates a timing signal in at least a portion of the VBI duration, which is supplied to an AND gate 220. The VID signal also is applied to time a counter 222 which is clocked by an oscillator circuit 224 to generate pulses substantially close to the horizontal sync phase and frequency of a video signal being supplied via an input 226 to a blanking circuit 228. A timing generator 230 is used to generate pulses that are within the HBI vicinity of the incoming video signal. Typically the pulse duration of the output of the generator 230 is in the range of 1 μ s to 10 μ s, with 4.7 μ s as one example. The output of the generator 218 is also used to blank or to replace some portion of the VBI via the blanking circuit 228. A combining circuit 232 is coupled at a negative input to the AND gate 220 and at a positive input to the blanking circuit 228, and is used to add back at least some regenerated sync pulses supplied by the timing generator 230. Thus an output 234 of the combining circuit 232 is a signal with substantially the same video signal outside the VBI vicinity but with some portions of the VBI modified, attenuated, or removed so as to alter the effects of an anti-copy protection signal (that is, the effects in a TV set and/or a VCR).

Although the invention has been described herein relative to specific embodiments, various additional features and advantages will be apparent from the description and

Abstract The purpose of this study was to determine the effect of a 12-week training program on the physical fitness of 10-year-old children. The study was conducted in a primary school in the city of Ankara, Turkey. The study group consisted of 20 children (10 boys and 10 girls) who were randomly selected from the 10-year-old children in the school. The children were divided into two groups: a control group and an experimental group. The control group did not participate in any physical education program, while the experimental group participated in a 12-week training program. The physical fitness of the children was measured at the beginning and at the end of the 12-week period. The measurements included heart rate, blood pressure, and body mass index. The results of the study showed that the experimental group had significantly higher heart rates and blood pressures at the end of the 12-week period compared to the control group. Additionally, the experimental group had a significantly lower body mass index at the end of the 12-week period compared to the control group. These findings suggest that a 12-week training program can improve the physical fitness of 10-year-old children.